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Remote p-Doping of InAs Nanowires

H.-Y. Li, O. Wunnicke,* M. T. Borgström, W. G. G. Immink, M. H. M. van Weert, M. A. Verheijen, and E. P. A. M. Bakkers

Philips Research Laboratories, High Tech Campus 4, 5656 AE Eindhoven, The Netherlands

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ABSTRACT

We report on remote p-type doping of InAs nanowires by a p-doped InP shell grown epitaxially on the core nanowire. This approach addresses the challenge of obtaining quantitative control of doping levels in nanowires grown by the vapor–liquid–solid (VLS) mechanism. Remote doping of III–V nanowires is demonstrated here with the InAs/InP system. It is especially challenging to make p-type InAs wires because of Fermi level pinning around 0.1 eV above the conduction band. We demonstrate that shielding with a p-doped InP shell compensates for the built-in potential and donates free holes to the InAs core. Moreover, the off-current in field-effect devices can be reduced up to 6 orders of magnitude. The effect of shielding critically depends on the thickness of the InP capping layer and the dopant concentration in the shell.

Semiconductor nanowires[1−3] enable monolithic integration of III−V semiconductors onto group IV substrates[4−6] to add new functionalities to the established silicon technology. For appropriate operation of electronic devices[7] like field-effect transistors (FETs) and opto-electronic components such as light-emitting diodes, quantitative control of impurity doping levels is required. So far, p-type as well as n-type doping of nanowires has been demonstrated qualitatively for, e.g., Si,[1] GaAs,[8] InP,[9,10] and GaN.[11,12]

However, for nanowires grown via the vapor−liquid−solid (VLS) mechanism at relatively low temperatures, it is not known whether impurity atoms interact with the metal particle and how they are incorporated into the semiconductor crystal. Furthermore, with decreasing nanowire diameter, the impurity ionization energy increases due to confinement.[13,14] It has recently been shown[15] that the nanowire growth mode can be switched from axial (VLS) to radial (film deposition) growth by an increase of the growth temperature. The conditions for radial growth are similar to conventional layer growth of bulk materials, for which the incorporation and activation of dopant atoms are well established. A possible way to obtain control of doping levels in nanowires is to synthesize core/shell structures, where the dopant atoms are in the shell that donates carriers to the undoped core, i.e., to remotely dope nanowires.[16] Remote doping has been widely employed in heteroepitaxial layers to obtain high-mobility two-dimensional electron gases.[17] Because of a conduction (valence) band offset between the semiconductors, the free electrons (holes) fall into the energy well of the undoped semiconductor. Thereby, they are spatially separated from the ionized impurities. This results in higher carrier mobilities as the strong scattering at ionized dopants in the channel is substantially reduced. Remote doping enables to predefine the amount and type of carriers in the conduction channel. Another method to create a high mobility carrier gas in nanowires is radial band structure engineering. It has been used in undoped core/shell nanowires.[18,19] However, the doping concentration cannot be controlled efficiently, and band structure engineering is limited to material combinations with suitable band alignments.

To demonstrate remote doping in III−V nanowires, we have chosen to remotely dope InAs nanowires by a p-doped InP shell. It is challenging to p-dope InAs nanowires because of surface Fermi level pinning around 0.1 eV above the conduction band edge for p- and n-type doping. This leads to a surface electron inversion layer with a low sheet resistance of around 1 kΩ.[20] For 1 μm long InAs nanowires with a diameter of 20 nm as we use here, this results in a resistance of only 17 kΩ. This surface leaking current causes a high off-current in field-effect transistor devices. The surface Fermi level pinning effect becomes more dominant for thin nanowires because of the long radial shielding lengths of the surface built-in potential. The shielding length can easily exceed the nanowire radius and thus determines the Fermi level in the whole nanowire.[21] So far, p-type doping of InAs nanowires with a high on−off ratio has not been reported. Here we demonstrate that we can effectively induce p-type doping in InAs core nanowires and reduce the surface current drastically. We have studied the effect of the InP shell thickness and acceptor concentration on the conductance properties of the intrinsic InAs core.

The InAs core nanowires were synthesized on an InP-(111)B substrate by metal-organic vapor-phase epitaxy

* Corresponding author. E-mail: olaf.wunnicke@nxp.com. Telephone: 0031-40-27-46289. Fax: 0031-40-27-43352. Current Adress: NXP Semiconductors, Research, High Tech Campus 4, 5656 AE Eindhoven, The Netherlands.

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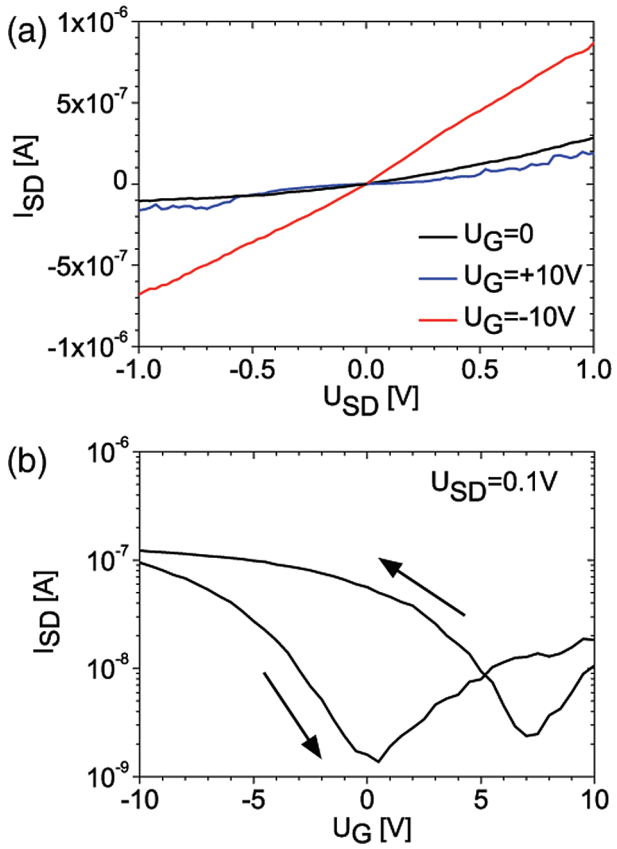

Figure 1. Electrical properties of bare p-doped InAs nanowires: (a) shows the *IV* curves at different gate voltages and (b) shows the transfer curve at 0.1 V source-drain voltage.

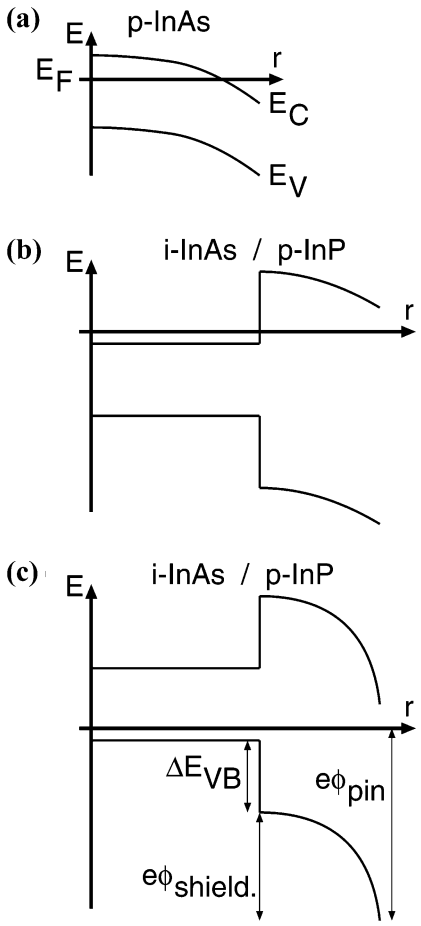

Figure 2. Schematic radial band diagrams at zero gate voltages. The valence (E_V) and conduction (E_C) band edges relative to the Fermi energy (E_F) are depicted. (a) Bare p-InAs nanowire. (b,c) An i-InAs core nanowire capped with a p-doped InP shell. In (b), the surface Fermi level pinning is not sufficiently shielded. (c) The optimum shielding of the built-in potential due to surface Fermi level pinning (ϕ_{pin}) by the ionized acceptors in the shell (ϕ_{shield}) and the valence band offset between InAs and InP (E_{VB}).

(MOVPE) at a temperature of 420 °C for 30 min. For bare p-InAs nanowires, diethylzinc was used as p-type dopant at a molar fraction of 5×10^{-5}. To obtain the core/shell nanowires, the temperature was increased under AsH_3 flow to 500 °C. Then the InP shell was deposited for 5 and 15 min by switching from AsH_3 to PH_3, resulting in a shell thickness of 7 and 20 nm, respectively. Diethylzinc was used during InP shell growth at a molar fraction of 1×10^{-5} (N_A^0) and 5×10^{-5} ($5N_A^0$). In the case of bulk growth conditions, N_A^0 would result in a hole concentration of 3.5×10^{18} cm^{-3}. Note that here the shell growth conditions differ from ordinary bulk growth. The nanowires were transferred onto a highly doped Si substrate provided with 130 nm dry thermally grown SiO_2 acting as the back-gate dielectric. Ti/Zn/Au contacts were defined by optical lithography and lift-off. Subsequently, rapid thermal annealing was carried out at 300 °C for 30 s to highly dope the contact regions by Zn indiffusion and to activate hydrogen passivated Zn in the p-InP shell.[22] The channel length of the nanowire field-effect transistor devices was varied between 0.5 and 5.0 μm. In total, 60 nanowire field-effect transistor devices were fabricated and characterized electrically at room temperature.

Figure 1a shows a typical *IV* characteristic of a bare p-doped InAs nanowire at different gate voltages (U_G). The two-point contact resistances at $U_G = -10$ V are on the order of 1 MΩ. Comparable resistances have been observed before for thin n-type InAs nanowires.[2,23] The small asymmetry is due to the different core thicknesses induced by tapering during the VLS growth. The gate effect is attributed to effects inside the nanowire and not to barrier height switching at the contacts as in common field-effect transistors. The transfer curve of this device in Figure 1b clearly shows ambipolar behavior. Furthermore, the transfer curve exhibits a large hysteresis that is discussed in more detail in the Supporting Information. At negative and zero gate voltages, the nanowire conducts the current mainly via free holes in the bulk of the nanowire. The current increase at positive gate voltages is attributed to the surface current carried by electrons.[20] This current limits the on−off ratio (measured at $U_G = \pm 10$ V) to typical values between 10 and 100. The radial band bending of the bare p-doped InAs nanowire at zero gate voltage is depicted schematically in Figure 2a. It shows that the Fermi level pinning determines the Fermi level in a large portion of the nanowire. Importantly, the inversion layer at the surface results in the high off-current and reduces the on-current due to hole depletion at the surface.

A statistical overview of the transfer characteristics for all measured devices is shown in Table 1. About 75% of the bare p-doped InAs nanowires (first row) exhibit bipolar

Table 1. Overview of the Measured Nanowire FETs[a]

N_A	t	behavior	R_{ON} [Ω]	R_{OFF} [Ω]	on−off	#
	bare	bipolar	$10^6..10^7$	$10^6..10^8$	10..100	15
N_A^0	7 nm	bipolar	$10^7..10^9$	$10^6..10^8$	1..10	8
$5N_A^0$	7 nm	bipolar	$10^5..10^7$	$10^6..10^{10}$	10..100	15
N_A^0	20 nm	p	$10^6..10^7$	$10^{10}..10^{12}$	$10^4..10^6$	11
$5N_A^0$	20 nm	p	$10^5..10^6$	$10^6..10^8$	1..10	11

[a] In the first and second column, the dopant concentration (N_A) and the thickness (t) of the p-InP shell is shown, respectively. The bare p-InAs nanowires are directly impurity doped. The third column shows the transfer curve behavior of the majority of devices. The fourth and fifth columns give the range of source-drain resistances at gate voltages of −10 V and +10 V, respectively. The last two columns show the on−off ratios and the total number of measured devices.

behavior. The rest of the devices show p-type character with low on−off ratios. The spread in the data, especially in the off-currents, is explained by the tapered diameter of the InAs nanowires from 20 to 40 nm. Recently, it has been reported that the electron current in InAs nanowires with diameters below 80 nm depends strongly on the diameter.[23] Our results show that it is not possible to induce p-type doping in thin, uncapped InAs nanowires with a favorably high on−off ratio.[24]

To remotely dope p-InAs wires and to suppress the surface electron current, the core is capped with a p-doped InP shell. A representative cross-sectional high-angle annular dark-field (HAADF) transmission electron microscopy (TEM) as well as a high-resolution TEM image of the InAs/InP core/shell nanowire are shown in parts a and b of Figure 3, respectively. In total, we have studied 20 NW cross-sections with TEM. The contrast in the HAADF image and the corresponding EDX line scan shows that the InAs core has a diameter of around 20 nm and is capped with an InP shell of thicknesses varying between 7 and 10 nm. Most probably this variation is induced by the local nanowire density on the substrate because the growth is diffusion-limited. The InAs/InP interface sharpness is below the lateral resolution of the EDX scan of around 3 nm. Furthermore, the shell exhibits a gradual transition from InAsP to InP due to Arsine carry-over[25] after VLS growth of the InAs core. High-resolution TEM imaging (Figure 3b) shows that the structure is free of dislocations. The core grows in the wurtzite structure along the [0001] direction and has nonpolar $\{11\bar{2}0\}$ side facets. This indicates that the gradual transition reduces the lattice strain for these mismatched materials. In addition, residual strain can be relieved in the radial direction for these thin nanowires.

Because the p-InP shell suffers from surface Fermi level pinning as well,[21] the built-in potential must be shielded by the ionized acceptors in the shell. The actual built-in potential (ϕ_{shield}) that must be shielded for optimum shielding (see Figure 2c) is the built-in potential due to the surface Fermi level pinning (ϕ_{pin}) minus the valence band offset between InAs and InP (E_{VB}): $e\phi_{shield} = e\phi_{pin} - E_{VB}$. If not done properly, the surface Fermi level pinning also leads to an electron inversion layer at the InAs/InP interface, as depicted schematically in Figure 2b. Furthermore, the band bending as shown in Figure 2b,c creates a large electric field that

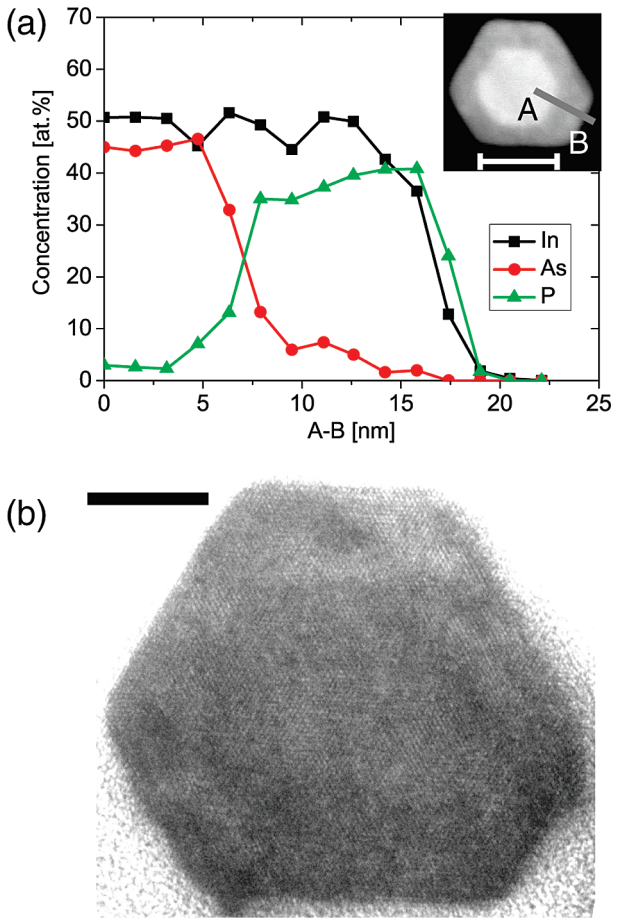

Figure 3. Cross-section transmission electron microscopy (TEM) study of a core/shell nanowire. In (a), an EDX scan is shown. Inset: high-angle annular dark-field (HAADF) TEM picture with the position of the EDX line scan. Scale bar: 20 nm. In (b), a high-resolution TEM picture of this core/shell nanowire is shown. Scale bar: 10 nm.

forces the free holes in the p-InP shell toward the InAs core. The band offset between InP and InAs of around 0.4 eV confines the holes inside the InAs core nanowire. To calculate the radial band bending, we assume cylindrical core/shell nanowires with an homogeneous ionized acceptor distribution in the shell and an undoped core nanowire. The surface defect density is assumed to be so high that the Fermi level is pinned at the defect levels. We have neglected the band bending in the thin InAs core because the Debye length is larger than the core radius. By solving the Laplace equation, a condition for optimum shielding of the surface built-in potential can be given by

$$eNt^2\left[1 + \frac{1}{3}\frac{t}{R} - \frac{1}{4}\frac{t^2}{R^2} + \cdots\right] = -2\epsilon_0\epsilon_r\phi_{bi} \qquad (1)$$

Here t, N, and ϵ_r are the thickness, the dopant concentration, and the dielectric constant of the shell. R is the radius of the core and $R \gg t$ is assumed in eq 1 because only then an analytical solution can be derived. For $R/t \rightarrow \infty$, the bulk solution is obtained. Assuming a 20 nm thick p-InP shell on a 20 nm diameter InAs core, a surface Fermi level pinning

level of $\phi_{pin} = 1.2$ V, and a valence band offset of $E_{VB} = 0.4$ eV, the dopant concentration in the shell has to be 4×10^{18} cm^{-3} for optimum shielding. At higher concentrations or thicker shells, the built-in potential is compensated and, in addition, free holes are donated to the i-InAs core. Here the solution is obtained by solving the equations numerically without using the assumption $R \gg t$. Importantly, the effect of shielding depends linearly on the dopant concentration, but quadratically on the thickness. Hence, control of the shell thickness is essential for the use in remote doping. We have studied remote doping using two different doping levels of N_A^0 and $5N_A^0$ as well as two different shell thicknesses of 7 and 20 nm.

When capping the i-InAs core nanowires with a 7 nm thin p-InP shell with a N_A^0 dopant concentration, the surface Fermi level pinning is only partially shielded by the ionized Zn acceptors. This leads to a leaking current at the InAs/InP interface as depicted in Figure 2b. The off-current (see Table 1) at +10 V gate voltage is as high as for bare p-InAs nanowires. By increasing the acceptor concentration in the thin shell to $5N_A^0$, the shielding effect of the ionized acceptors is stronger, leading to a lower electron density at the interface and thus a lower off-current. However, because of the variation in shell thickness, some devices with a thin shell and a high dopant concentration show a very low off-current of 10^{-11} A, indicating that the built-in potential is nearly compensated. As shown in eq 1, the shielding depends quadratically on the shell thickness. This explains the much larger spread in the off-currents compared to the on-currents for these samples.

The case of optimum shielding is achieved by capping the i-InAs nanowires with a 20 nm thick p-InP shell with an acceptor concentration of N_A^0. In Figure 4a, the *IV* characteristic is shown. Because of the depleted InP shell, the two-point contact resistance has increased compared to bare p-InAs nanowires. The transfer characteristic in Figure 4b shows p-type behavior with a typical on-current in the range of 10 nA and an off-current below the noise level of our measurement setup (0.1 pA). All of these core/shell nanowire FETs exhibited p-type behavior with a very high on−off ratio between 10^4 and 10^6. Compared with bare p-doped InAs nanowires, the off-current is up to 6 orders of magnitude lower whereas the on-current is only slightly affected. This low off-current can only be achieved by effectively shielding the donorlike surface defects by ionized Zn acceptors in the p-InP shell. The free holes are forced into the InAs nanowire due to the electric field (band bending) inside the p-InP shell, as shown schematically in Figure 2b,c and calculated with eq 1. In the transfer curve of the capped nanowires, a large hysteresis is present which is believed to originate from water dipoles[26] (see fast gate-sweep measurements in the Supporting Information). This effect is not shielded by the p-InP shell. From the fast gate-sweep measurements, the hole mobility is estimated to around 20 cm^2 V^{-1} s^{-1}, which is a factor of 5 lower than reported hole mobilities for bulk zinc-blende InAs[27] but a factor of 2 higher than recently reported hole mobilities of passivated bare p-InAs nanowires.[24] As a comparison, the reported electron mobility in n-type InAs

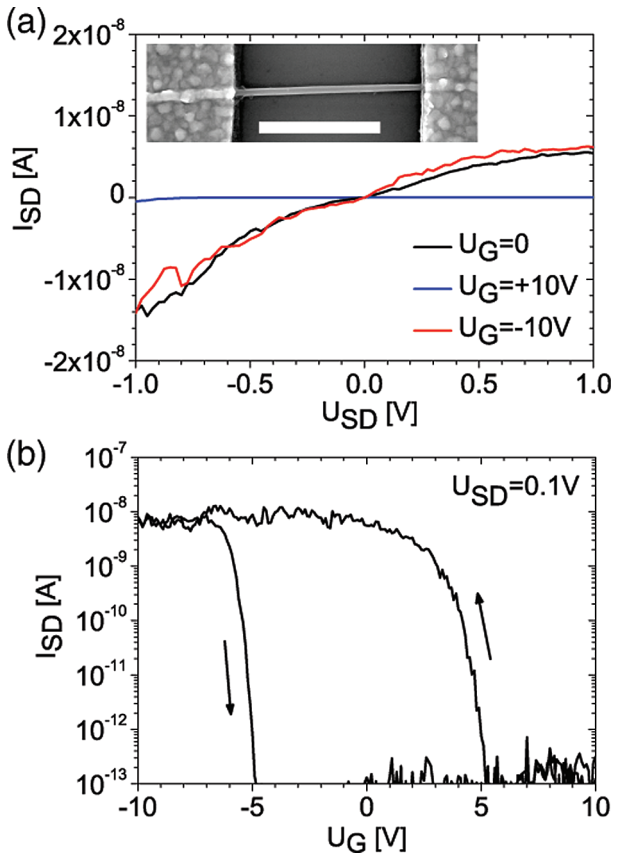

Figure 4. (a) *IV* curve and (b) transfer curve of a 20 nm diameter i-InAs nanowire capped with a N_A^0 p-doped 20 nm thick InP shell. The *IV* curves are taken at different U_G. The high current at $U_G = 0$ V shows that the device is a normally on p-FET. Inset: SEM image of nanowire FET. Scale bar: 1 μm.

NWs is typically 10−30 times lower than that of bulk InAs.[28,29] Here we have determined numerically[30] the gate capacitance of the back-gated core/shell nanowire FET. From the hole mobility and on-resistances, the hole density in the i-InAs core is estimated to be 10^{18}−10^{19} cm^{-3}. Here a 1 μm long and 20 nm diamter core nanowire is assumed. Note that the measured mobility is reduced by hysteresis due to slow relaxation and shielding of the gate voltage (see Supporting Information). We strongly believe that the hole mobility can be increased by passivating the InP surface and by improving our nonoptimized core/shell nanowires. This can, for instance, be achieved by inserting an intrinsic InP layer at the interface to separate the free holes from the ionized acceptors even more.

For wires with a thick p-InP shell and a $5N_A^0$ p-doping, the on-current exceeds that of the bare p-InAs nanowires, but the on−off ratio is drastically reduced (see Table 1). This shows that we can highly p-dope the InAs core such that depletion of the nanowires becomes difficult. However, we cannot exclude that, in this case, the current is also conducted partially via free holes in the p-InP shell.

We should note that, from these experiments, we cannot exclude the possibility of Zn diffusion through the core/shell stucture during the deposition of the shell at higher temperatures.[31] However, from the strong reduction of the off-currents by capping the InAs core with a p-InP shell (see

Table 1), we believe that the largest fraction of the Zn atoms will stay inside the p-InP shell.

We have demonstrated remote doping in III−V semiconductor nanowires by epitaxially capping intrinsic InAs wires with a p-doped InP shell. Transport measurements show that we induced p-type doping in InAs and that the hole concentration in the InAs can be tuned by variation of the dopant concentration and the thickness of the shell. Moreover, the surface leakage current is effectively reduced by the capping, resulting in a dramatic increase of the on−off ratio.

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Supporting Information Available: Reduced hysteresis gate-sweep measurements. This material is available free of charge via the Internet at http://pubs.acs.org.

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